What Is Claimed Is:

1. A method for switching between at least two operating modes (SM, LM) of a processor unit (100, 101) comprising at least two execution units (ALUA, ALUB) for running programs (P1, P2, P3),
wherein at least one identifier (K2) is assigned to at least the programs (P1, P2, P3), the identifier allowing a differentiation between the at least two operating modes (SM, LM), and switching between the operating modes being performed as a function of the identifier (K1-K4, KB) such that the processor unit (100, 101) runs the programs (P1, P2, P3) according to the assigned operating mode.

2. The method as recited in Claim 1,
wherein the programs (P1, P2, P3) contain task programs (AP) or constitute them, and the identifier (K1) is assigned to the corresponding individual task programs (AP).

3. The method as recited in Claim 1,
wherein the programs (P1, P2, P3) are made up of individual program segments (CB) or contain them, and the identifier (K3) is assigned to the corresponding individual program segments (CB).

4. The method as recited in Claim 1,
wherein the programs (P1, P2, P3) are made up of individual program instructions (PB), and the identifier (K4) is assigned to the corresponding individual program instructions (PB).

5. The method as recited in Claim 1,
wherein the programs (P1, P2, P3) are part of an operating system of the processor unit (100, 101) or constitute the operating system.

6. The method as recited in Claim 1,
wherein the programs (P1, P2, P3) are used for controlling operating sequences of a vehicle.

7. The method as recited in Claim 1,
wherein a first operating mode is provided which corresponds to a safety mode (SM)

in which the two execution units (ALUA, ALUB) run identical programs (AP, P2) redundantly.

8. The method as recited in Claim 7,
wherein conditions or results (ResultA, ResultB) obtained while the programs (AP, P2) are run are compared (14) for agreement, errors being detected if there is a discrepancy.

9. The method as recited in Claim 7,
wherein the programs (AP, P2) are run synchronously.

10. The method as recited in Claim 1,
wherein in the second operating mode, which corresponds to a performance mode (LM), each execution unit (ALUA, ALUB) runs different programs (P1, P2, P3).

11. The method as recited in Claim 1,
wherein the identifier (K1, KB) is in the form of at least one bit (K1/B1).

12. The method as recited in Claim 1,
wherein a program instruction (PB1, PB2, PB3) is provided that generates an identifier (KB) indicating if the program is to be run in the first or second operating mode.

13. The method as recited in Claim 1,
wherein the identifier (KB) is written to a specific memory area (SSB).

14. The method as recited in Claim 12 or 13,
wherein the identifier (KB) is generated by an instruction (PB1, PB2) provided in an instruction set of the processor unit.

15. The method as recited in one of Claims 12 through 14,
wherein the identifier (KB) is generated by a write instruction (WR).

16. A device for switching between at least two operating modes (LM, SM) of a processor unit (100, 101) for running programs (P1, P2, P3) comprising at least two execution units (ALUA, ALUB), switching means (8, 9) being included, via which switching can be performed,

wherein these switching means (8, 9) assign at least one identifier (K1-K4, KB) to at least the programs (P1, P2, P3), the identifier allowing a differentiation between the two operating modes (LM, SM), and the switching means (8, 9) being designed in such a way that they switch between the operating modes as a function of the identifier, and the processor unit runs the programs according to the assigned operating mode.

17. The device as recited in Claim 16,
wherein at least duplicate arithmetic-logic units (ALUA, ALUB) are provided correspondingly as at least two execution units.

18. A processor unit (100, 101) for running programs (P1, P2, P3) comprising at least two execution units (ALUA, ALUB), switching means (8, 9) being included, via which it is possible to switch between at least two operating modes (LM, SM) of the processor unit,
wherein these switching means (8, 9) assign at least one identifier (K1-K4, KB) to at least the programs (P1, P2, P3), the identifier allowing a differentiation between the two operating modes (LM, SM), and the switching means (8, 9) being designed in such a way that they switch between the operating modes as a function of the identifier, and the processor unit runs the programs according to the assigned operating mode.